

In the Claims:

Please enter the following amended claims 1, 4-5, 9, 12, 14, 17, 20, and 23:

c1
1. (Twice Amended) A method comprising steps of:

forming a layer over a transistor gate region and a field oxide region;

forming a doping barrier above said layer over said field oxide region;

doping said layer over said transistor gate region with a dose of a first dopant,

wherein said dose of said first dopant is a dosage greater than required to result in said
layer over said transistor gate region having transistor gate electrical properties;

removing said doping barrier;

doping said layer over said transistor gate region and said field oxide region with a
second dopant so as to form a high resistivity resistor in said layer over said field oxide
region without affecting said transistor gate electrical properties.

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4. (Once Amended) The method of claim 1 wherein said transistor gate region is a
gate of an PFET.

5. (Once Amended) The method of claim 1 wherein said transistor gate region is a
gate of an NFET.

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9. (Once Amended) The method of claim 1 wherein said first dopant comprises

c³
phosphorous at a dose of approximately 6.5×10^{15} atoms per square centimeter.

c⁴
12. (Once Amended) The method of claim 1 wherein said second dopant comprises boron at a dose of approximately 1.0×10^{15} atoms per square centimeter.

14. (Twice Amended) A method comprising steps of:
depositing a polycrystalline silicon layer on a chip, said polycrystalline silicon layer including a gate region and a resistor region;
forming a doping barrier above said polycrystalline silicon layer so as to prevent doping of said resistor region of said polycrystalline silicon layer;
doping said polycrystalline silicon layer with a dose of a first dopant, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said gate region having transistor gate electrical properties;
removing said doping barrier;
doping said polycrystalline silicon layer with a second dopant so as to form a high resistivity resistor in said resistor region of said polycrystalline silicon layer without affecting said transistor gate electrical properties.

c⁶
17. (Twice Amended) The method of claim 14 wherein said step of doping said polycrystalline silicon layer with a first dopant comprises doping said gate region.

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20. (Once Amended) The method of claim 14 wherein said first dopant comprises phosphorous at a dose of approximately 6.5×10^{15} atoms per square centimeter.

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23. (Once Amended) The method of claim 14 wherein said second dopant comprises boron at a dose of approximately 1.0×10^{15} atoms per square centimeter.